Chapter 2: Automatic distribution of Lustre and Esterel synchronous programs

Alain Girault
(Joint work with Paul Caspi)
(and with Clément Ménier for circuits)

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Outline

1 Context and overview
2 The different distribution approaches
3 OC code distribution
4 SC code distribution
5 CP code distribution

Context

Embedded and reactive systems are distributed:
- physical location of sensors and actuators
- fault-tolerance
- performance improvement

In general, distribution is driven by the user

Synchronous programming languages are concurrent
Embeedded and reactive systems are distributed:
- physical location of sensors and actuators
- fault-tolerance
- performance improvement

In general, distribution is driven by the user

Synchronous programming languages are concurrent

But:

\[ \text{expression parallelism} \neq \text{execution parallelism} \]

Asynchronous parallel programming languages

E.g.: Ada, Occam, multi-threaded Java, ...

Advantages
- global view
- debugging on the source code

Inconvenients
- the interleaving semantics is non-deterministic
- debugging must be performed on non-deterministic sequential object code

Synchronous parallel programming languages

E.g.: Esterel, Lustre, Signal/Polychrony, Heptagon, Prelude, ...

Advantages
- global view
- debugging on the source code
- debugging on deterministic sequential object code

Inconvenients
- how to generate distributed code?

[E.A. Lee, The problem with threads]
Automatic distribution

To benefit from the advantages of synchronous programming, one must generate **automatically** the corresponding distributed code.

![Diagram: Source program \(\rightarrow\) Automatic distributor \(\rightarrow\) Distribution specifications \(\rightarrow\) Distributed program]

**Distribution specifications:** \(N\) computing locations \(\rightarrow\) partition of the set of inputs/outputs into \(N\) subsets.

Driven by the physical location of the sensors and actuators (We do not seek the best performances nor the maximal parallelism)

---

Direct source code distribution (1)

**Algorithm**
- Cut the source program into \(N\) fragments
- Compile **separately** each fragment
- Make the \(N\) fragments communicate harmoniously

This is the ideal solution

---

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Direct source code distribution (1)

Algorithm
- Cut the source program into $N$ fragments
- Compile separately each fragment
- Make the $N$ fragments communicate harmoniously

This is the ideal solution

But in general it does not work

A counter-example (1)

node MAIN (I1:int) returns (O2:int);
var O1,I2:int;
let
O1 = I1;
O2 = I2;
I2 = O1;
tel;

A counter-example (2)

Compiling a concurrent program (e.g., Lustre) into sequential code means sequentializing it!

The red fragment can be sequentialized in two ways:

```
<table>
<thead>
<tr>
<th>main program</th>
<th>blue fragment</th>
<th>red fragment</th>
</tr>
</thead>
<tbody>
<tr>
<td>O2:=I1;</td>
<td>I2:=01;</td>
<td>01:=I1;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>02:=I2;</td>
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<td>O1:=rcv(R);</td>
<td>02:=I2;</td>
</tr>
<tr>
<td></td>
<td>I2:=01;</td>
<td>I2:=rcv(B);</td>
</tr>
<tr>
<td></td>
<td>snd(R,I2);</td>
<td>O2:=I2;</td>
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<td>01:=rcv(R);</td>
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<tr>
<td>I2:=01;</td>
<td></td>
<td>snd(B,01);</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I2:=rcv(B);</td>
</tr>
<tr>
<td></td>
<td></td>
<td>02:=I2;</td>
</tr>
<tr>
<td>02:=I1;</td>
<td>I2:=01;</td>
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</tr>
<tr>
<td></td>
<td></td>
<td>01:=I1;</td>
</tr>
</tbody>
</table>

Direct source code distribution (2)

Algorithm

- Cut the source program into $N$ fragments
- For each fragment 1 to $N$:
  - compile fragment $i$, taking into account the scheduling constraints $C_1$ to $C_{i-1}$
  - synthesize the scheduling constraints $C_i$ for the next fragments

Solution adopted in *Signal*

The code distribution algorithm must perform the causality analysis at the same time as the distribution

Problem: in which order must the fragments be compiled?
The source program is debugged first
The causality analysis is performed by the compiler
The method can be common to several synchronous languages

Common format to the Lustre and Esterel compilers
Finite state automaton with a DAG of actions in each state
One reaction of the program = one transition of the automaton
Purely sequential control flow
Explicit and static control structure

Output format of the Esterel compiler
Sequential circuit with a finite memory to drive a table of actions on data types
One reaction of the program = one clock cycle of the circuit
Parallel control flow
Implicit and dynamic control structure
Opens up possibilities to do hardware/software codesign
Structure of the OC code

An OC program handles **signals** and **variables**:
- **signal** = input/output of the source program
- **variable** = associated to **valued** signals and local variables

The nodes of the DAG can be:
- **Root**: Implicit read of the input signals
- **Unary node**:
  - Variable assignment: \( x := \text{exp} \)
  - Output signal emission: \( \text{output } y \)
  - External procedure call: \( \text{call } p \)
- **Binary node**: binary test: \( \text{if, present} \)
- **Leaf**: change state: \( \text{goto } s \)

A running example in OC

```oc
input ck,x:integer;
output y,z:integer;

State 0

go(ck,x);
if (ck) then
  y:=calcul(x);
  output(y);
else
  z:=x;
  output(z);
endif

goto 0;
```

Distribution directives

The user wants \( N \) computing sites
- **Partition** of the set of inputs/outputs of the program into \( N \) subsets \( V_i \) \((i = 1..N)\)

Running example:
- Site 0: \( V_0 = \{ck, x, z\} \)
- Site 1: \( V_1 = \{y\} \)

OC distribution algorithm

1. Duplicate the sequential code on each computing location
2. Assign a location to each variable and action
3. On each computing location, do:
   1. Prune useless actions
   2. Insert communications
   3. Insert synchronizations

Classical notations:
- \( \text{use}(A) = \{\text{variables used by node } A\} \)
- \( \text{def}(A) = \{\text{variables modified by node } A\} \)
The OC running example

State 0

```plaintext
go(ck,x);
if (ck) then
    y:=calcul(x);
    output(y);
else
    z:=x;
    output(z);
endif

goto 0;
```

State 0 – Site 1

```plaintext
go(ck,x);
if (ck) then
    y:=calcul(x);
    output(y);
else
    z:=x;
    output(z);
endif

goto 0;
```

Inter-cite data dependencies!
Í Need to insert communications.
The OC running example

State 0 – Site 0

go(ck,x);
if (ck) then
else
z:=x;
output(z);
endif
goto 0;

State 0 – Site 1

if (ck) then
y:=calcul(x);
output(y);
else
endif
goto 0;

Inter-cite data dependencies!

Choice of the communication primitives

Rendezvous (Ada, OCCAM)

- asynchronous but synchronizing
- incur unnecessary delays

FIFOs

- truly asynchronous
- send and receive delayed
- send and receives must be performed in the same order

Communication insertion algorithm

Sends

Compute at each node of the DAG the sets $E_{need}^s$ of variables needed by $s$:

1. Traverse the DAG backward starting from the leaves
2. For each $x \in \text{use}(A)$, if $x \notin V_s$ then $E_{need}^s := E_{need}^s \cup \{x\}$
3. For each $y \in \text{def}(A)$, if $y \in E_{need}^s$ then insert a $\text{snd}(s,x)$ in the DAG of site $t$

Receives

Compute at each node of the DAG the ordered sets $Q_{fifo}^{(s,t)}$ of variables sent by $s$ to $t$:

1. Traverse the DAG forward starting from the root
2. For each $\text{snd}(t,x)$ insert $x$ in $Q_{fifo}^{(s,t)}$
3. For each $x \in \text{use}(A)$, if $x \notin V_s$ then insert a $x:=\text{rcv}(s)$ in the DAG of site $t$

Communication primitives

Send

- $\text{snd}(j,x)$ insert value $x$ in the FIFO connected to site $j$
- non-blocking
- (could be blocking when FIFO is full for synchronization)

Receive

- $y:=\text{rcv}(i)$ extracts the head value from the FIFO connected to site $i$ and assigns it to variable $y$
- blocking when the FIFO is empty
The OC running example

State 0 – Site 0

```plaintext
go(ck,x);
if (ck) then
  snd(1,x);
else
  z:=x;
  output(z);
endif
goto 0;
```

State 0 – Site 1

```plaintext
ck:=rcv(0);
if (ck) then
  x:=rcv(0);
  y:=calcul(x);
  output(y);
else
  z:=x;
  output(z);
endif
goto 0;
```

Resynchronization

One computing location could be purely a producer of values for another location (e.g., site 0)

- Can lead to unbounded FIFOs

The initial centralized program follows a notion of cycle / reaction (= one transition of the OC automaton)

- What is the meaning in the distributed case?
Resynchronization

One computing location could be purely a producer of values for another location (e.g., site 0)

- Can lead to unbounded FIFOs

The initial centralized program follows a notion of cycle / reaction (= one transition of the OC automaton)

- What is the meaning in the distributed case?

Resynchronization methods:
- **Strong** resynchronization
- **Weak** resynchronization

Weak synchronization

- At most one time lag between any pair of computing locations

**Weak “total” synchronization:**
- At least one message exchange between any two locations at each reaction
- Built upon the existing sends and receives

Strong synchronization

- No delay at all between any two computing location:
  - All computing location must execute synchronously the same automaton reaction
  - A synchronization must occur at the end of each reaction

  - A token circulating twice between all N nodes: $2 \times N$ synchronization messages
  - A rendezvous between all N nodes: $N \times (N-1)$ synchronization messages

**Weak “total” synchronization:**
- At least one message exchange between any two locations at each reaction
- Built upon the existing sends and receives

**Weak “if needed” synchronization**
- Only between locations that already communicate with each other
- Only during the reactions where they do communicate
Weak synchronization

At most one time lag between any pair of computing locations

Weak "total" synchronization:
- At least one message exchange between any two locations at each reaction
- Built upon the existing sends and receives

Weak "if needed" synchronization
- Blocking snd to implement bounded capacity FIFOs
- Relaxed form of resynchronization where there can be N time lags

The OC running example

State 0 – Site 0

```plaintext
go(ck,x);
snd(1,ck);
if (ck) then
  snd(1,x);
else
  z:=x;
  output(z);
endif
rcv_void(1);
goto 0;
```

State 0 – Site 1

```plaintext
goto 0;
```

State 0 – Site 0

```plaintext
go(ck,x);
snd(1,ck);
if (ck) then
  snd(1,x);
else
  z:=x;
  output(z);
endif
rcv_void(1);
goto 0;
```

State 0 – Site 1

```plaintext
ck:=rcv(0);
if (ck) then
  x:=rcv(0);
y:=calcul(x);
  output(y);
else
  z:=x;
  output(z);
endif

goto 0;
```
Discussion

Benefits:
- It works
- There is a formal correctness proof [Caillaud, Caspi, et al, 1994], based on semi-commutations and transition systems labelled with partial orders

Drawbacks:
- The OC automaton must be generated first, which suffers from the well known state space explosion
- The distribution is strict: all the computing locations must have the same rate
- The communications must be lossless

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Automatic Production of Globally Asynchronous Locally Synchronous Systems

Alain GIRAULT INRIA Rhône-Alpes
and
Clément MÉNIER ENS Lyon
GALS Systems

Acronym for “Globally Asynchronous Locally Synchronous”

In software: paradigm for composing blocks and making them communicate asynchronously

In hardware: circuits designed as sets of synchronous blocks communicating asynchronously

No need to distribute the clock $\implies$ saves power

Our goal: automatically obtain GALS systems from a centralised program

Automatically Distributed Programs

Why distribute?

$\checkmark$ physical constraints, fault-tolerance, performance...

Advantages of automatic distribution:

$\checkmark$ less error-prone than by hand

$\checkmark$ possibility to debug & validate before distribution

$\checkmark$ ...

Related Work

The closest is Berry & Sentovich’2000:

“Implementation of constructive synchronous circuits as a network of CFSMs in POLIS”

Main differences with our work:

1. Partitioning of the circuit into N clusters is by hand
   
   Our partitioning is automatic

2. They partition the circuit, that is the control part
   
   We partition the data part and replicate the control part
Program Model: Synchronous Circuits (1)

Program = synchronous sequential circuit driving a table of actions

A control part and a data part:

- Control part = synchronous sequential boolean circuit
- Data part = table of external actions
  - manipulate inputs, outputs, and typed variables (integers, reals...)

A program has a set of input and output signals

Signals can be pure or valued

Valued signals are associated to a local typed variable

It can be obtained from Esterel -> so called SC internal format

VHDL code can be generated from it

The basic elements of SC circuits:

- standard: computes a Boolean expression (regular gates of the circuit)
- action: triggers an action from the table (the control is passed)
- ift: triggers a test from the table and assigns to the wire the result of the test
- input: takes the value of the presence Boolean of the signal and updates the value of the associated variable (if the input is valued)
- output: triggers an output action from the table
- register: a latch with an initial value

The circuit registers

The encode the internal state of the circuit:

- One boot register
- One loop register
- Several regular registers

A valuation of the register vector corresponds to one state of the OC automaton

A reaction of the program is one clock cycle

There are several control paths

Program Model: Properties

The control structure is:

- Parallel: there are several control paths
- Implicit: the state is coded in the registers
- Dynamic: the control depends on the data

Important property: any given variable can only be modified in one parallel branch (same as in Esterel)
Control structures

Exactly like a binary branching (so dealt with as before)

It is not possible to tell in which order the actions are performed

Impossible to simulate at compile-time the state of the FIFO queues
to insert the receive operations

One FIFO per variable

Distribution Method

1. Design a centralised system

2. Compile it into a single synchronous circuit

3. Distribute it into $N$ communicating synchronous circuits

We focus here on the point 3: the automatic distribution

Distribution Specifications

Must be provided by the user:

- The desired number of computing locations

- The localisation of each input and output

  derived from the physical localisation of the sensors and actuators

An Example: FOO

```
input I1; ift PI1
N1 := 0
N2 := 0
emit O1(N1)
N2 := N2 + 1
input I2; ift PI2
N1 := N1 + 1
emit O1(N1)
N2 := N2 * N1
emit O2(N2)
```

```
input I1; ift PI1
N1 := N1 + 1
input I2; ift PI2
N2 := N2 + 1
N2 := N2 * N1
emit O2(N2)
N1 := N1 + 1
```
Distribution Specifications of FOO

Where are we Heading?

Distribution Algorithm: Principle

Based on past work: Caspi, Girault, & Pilaud’1999

- **Replicate** the control part and **partition** the data part

1. **Localise** each action to get \( N \) virtual circuits
2. **Solve** the distant variables problem for each virtual circuit
3. **Project** each virtual circuit to get one actual circuit
4. **Solve** the distant inputs problem

We obtain \( N \) circuits communicating harmoniously ✷ without inter-blocking and with the same functional behaviour

Communication Primitives

Asynchronous communications

- Two FIFO queues associated with each pair of locations and each variable

- Each queue is identified by a triplet \( \langle \text{src}, \text{var}, \text{dst} \rangle \)

Two communication primitives:

- On location \( \text{src} \): \text{send}(\text{dst},\text{var})** non blocking**

- On location \( \text{dst} \): \text{var}:=\text{receive}(\text{src},\text{var})** blocking when empty**
Localisation of the Actions

Only the data part is partitioned: the control part is replicated.

<table>
<thead>
<tr>
<th>loc.</th>
<th>action</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>input I1; ift PI1</td>
</tr>
<tr>
<td>M</td>
<td>input I2; ift PI2</td>
</tr>
<tr>
<td>M</td>
<td>N1 := 0</td>
</tr>
</tbody>
</table>

Two Problems to Solve

1. Distant variables problem:
   - Not computed locally
   - We add send and receive actions

2. Distant inputs problem:
   - Not received locally
   - But: input signals convey two informations: value and presence
   - And: an ift net is required to modify the control flow according to the input's presence
   - We add input simulation blocks

Solving the Distant Variables Problem

We apply a simple algorithm to solve the data dependencies to each buffered path (sequential path):

1. Isolate a buffered path and mark its root and tail
2. Insert the send actions in the buffered path
   - Traverse the path backward to insert the send actions asap
3. Insert the receive actions in the buffered path
   - Traverse the path forward to insert the receive actions alap
4. Proceed to the unmarked successor nets of the tail

Partial Result for FOO

This is still one circuit representing two virtual circuits

The next step is to project onto two actual circuits
Solving the Distant Inputs Problem

Reminder: input signals convey two informations: the value and the presence.

And: an ift net is required to modify the control flow according to the input's presence.

Our goal is to send the presence information only to those computing locations that need them:

1. Detect the impure input-dependent nets and their needed inputs
   - Circuit traversal to compute for each net the set $S_{Input} = \{\text{needed inputs}\}$

2. Create the simulation blocks for the input nets

3. Connect the nets detected at step 1 to the required simulation blocks
On all $M$ such that $I \notin M$

On the $L$ such that $I \in L$

Creation of the Input Simulation Blocks

Connection of the Input Simulation Blocks
Connection of the Input Simulation Blocks

\[
\text{Visited} \land \text{SInput} = \emptyset \{ \\
\text{Visited} \lor \text{SInput} \neq \emptyset \{ \\
\text{SInput} = \{A, B\}
\]

Connection of an OR gate is similar

\[
\text{Visited} \lor \text{SInput} = \emptyset \{ \\
\text{Visited} = \{A, B\}
\]

Conclusion

This methods is interesting only if the data part is \textit{big} (because the control part is replicated)

Open directions : hardware/software codesign, post-distribution optimisations, ...

The most interesting perspective is to mix this approach with \textit{Berry & Sentovich’2000}:

- Accepting as inputs cyclic constructive circuits
- Automatic partitioning of the circuit into \(N\) clusters
- Partitioning both the data part and the control part

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Modern compiling methods for Esterel

- [Weil, Bertin, Closse, Poize, Venier & Pulou, CASES’00]
- [Edwards, CODES’99]
- [Potop, PhD’02] and [Potop, Edwards & Berry, 2007]

Common principle
- Linked list of control points
- Each control point is attached to a block of sequential code
- At each reaction, the list is traversed to execute only the active control points
- A sequential block can activate another block, but only further in the list or for the next reaction

**Distribution algorithm of CPREP**

1. Replicate the control structure (exe and pause vectors) onto each computing location

**Distribution algorithm of CPREP**

1. Replicate the control structure (exe and pause vectors) onto each computing location

2. Apply the OCREP algorithm to the DAG of each tâche $i$
Distribution algorithm of CPREP

1. Replicate the control structure (exe and pause vectors) onto each computing location

2. Apply the OCREP algorithm to the DAG of each tâche $i$

Works within the SAXO-RT compiler (FTR&D), after the control points have been computed

The communication mechanism is the same as with OCREP: FIFO queues

Technology transfer contract with FTR&D
Chapter 3

Automatic rate desynchronisation of reactive embedded systems

Alain GIRAULT

(Joint work with Paul CASPI, Xavier NICOLLIN, Daniel PILAUD, and Marc POUZET)

INRIA Grenoble Rhône-Alpes

Introduction

Embedded reactive programs

- **embedded** so they have limited resources
- **reactive** so they react continuously with their environment

We consider programs whose control structure is a finite state automaton

Put inside a periodic execution loop:

```
loop each tick
  read inputs
  compute next state
  write outputs
end loop
```

Automatic rate desynchronisation

**Desynchronisation:** to transform one centralised synchronous program into a GALS program

- Each local program is embedded inside its own periodic execution loop

**Automatic:** the user only provides distribution specifications

**Rate desynchronisation:**

- the periods of the execution loops will not be the same and
- not necessarily identical to the period of the initial centralised program
Motivation: long duration tasks

Characteristics:
- Their execution time is long
- Their execution time is known and bounded
- Their maximal execution rate is known and bounded

Examples:
- The CO3N4 nuclear plant control system of Schneider Electric
- The Mars rover pathfinder

A small example

Consider a system with three independent tasks:
- Task A performs slow computations:
  - duration = 8, period = deadline = 32
- Task B performs medium and not urgent computations:
  - duration = 6, period = deadline = 24
- Task C performs fast and urgent computations:
  - duration = 4, period = deadline = 8

How to implement this system?

Manual task slicing

Tasks A and B are sliced into small chunks, which are interleaved with task C

Very hard and error prone because:
- The slicing is complex
- The implementation must be correct and deadlock-free
Manually programming 3 async. tasks

Tasks A, B, and C are performed by one process each.

The task slicing is done by the scheduler of the underlying RTOS.

But the manual programming is difficult.

Example: the Mars Rover Pathfinder had priority inversion!

Automatic distribution

The user programs a centralised system.

The centralised program is compiled, debugged, and validated.

It is then automatically distributed into three processes.

The correctness ensures that the obtained distributed system is functionnally equivalent to the centralised one.

Example: the FILTER program

state 0:
go(CK, IN)
if (CK) then
  RES:=0
  write(RES)
  V:=0
  OUT:=SLOW(IN)
  write(OUT)
  goto 1
else
  RES:=V
  write(RES)
  goto 0
endif

state 1:
go(CK, IN)
if (CK) then
  RES:=OUT
  V:=OUT
  OUT:=SLOW(IN)
  write(OUT)
else
  RES:=V
  goto 1
endif
else
  RES:=V
  write(RES)
  goto 0
endif
Example: the **FILTER** program

**state 0:**
go(CK,IN)
if (CK) then
RES:=0
write(RES)
V:=0
OUT:=SLOW(IN)
write(OUT)
else
RES:=V
dendif
write(RES)
goto 1
endif

**state 0:**
go(CK,IN)
if (CK) then
RES:=0
write(RES)
V:=0
OUT:=SLOW(IN)
write(OUT)
else
RES:=V
dendif
write(RES)
goto 1
endif

**state 1:**
go(CK,IN)
if (CK) then
RES:=0
write(RES)
V:=0
OUT:=SLOW(IN)
write(OUT)
else
RES:=V
dendif
write(RES)
goto 1
endif

It has two inputs (the Boolean **CK** and the integer **IN**) and two outputs (the integers **RES** and **SLOW**)

It has two inputs (the Boolean **CK** and the integer **IN**) and two outputs (the integers **RES** and **OUT**)

**Rates**

The **FILTER** program has two inputs (the Boolean **CK** and the integer **IN**) and two outputs (the integers **RES** and **SLOW**)

Each input and output has a **rate**, which is the sequence of logical instants where it exists

- **IN** is used only when **CK** is **true**, so its rate is **CK**
- **CK** is used at each cycle, so its rate is the **base rate**
- **OUT** is computed each time **CK** is **true**, so its rate is **CK**
- **RES** is computed at each cycle, so its rate is the base rate

The **go(CK,IN)** action materialises the **read input phase**
A run of the centralised FILTER

\[
\begin{align*}
\text{IN}_1 &= 13 \\
\text{OUT}_1 &= 42 \\
\text{IN}_2 &= 9 \\
\text{OUT}_2 &= 27 \\
\end{align*}
\]

\[
\begin{align*}
\text{RES}_1 &= 0 \\
\text{RES}_2 &= 0 \\
\text{RES}_3 &= 0 \\
\text{RES}_4 &= 0 \\
\end{align*}
\]

\[
\begin{align*}
\text{CK}_1 &= T \\
\text{CK}_2 &= F \\
\text{CK}_3 &= F \\
\text{CK}_4 &= T \\
\end{align*}
\]

\[\text{WCET(SLOW)} = 7 \quad \text{WCET(other computations)} = 1 \]

\[\implies \text{WCET(FILTER)} = 8\]

Thus the period of the execution loop (base rate) must be greater than 8

Where are we going?

Two tasks running on a single processor:

Task L performs the fast computations
Task M performs the slow computations, sliced into 3 chunks
Where are we going?

Two tasks running on two processors:

Communication primitives

Two FIFO channels for each pair of locations, one in each direction:

- `send(dst, var)` inserts the value of variable `var` into the queue directed towards location `dst`

  Non blocking

- `var:=receive(src)` extracts the head value from the queue starting at location `src` and assigns it to variable `var`

  Blocking when the queue is empty

Distribution specifications

<table>
<thead>
<tr>
<th>location name</th>
<th>assigned rates</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>base</td>
</tr>
<tr>
<td>M</td>
<td>CK</td>
</tr>
</tbody>
</table>

This part is given by the user

Our automatic distribution algorithm

One centralized automaton

Automatic distributor

Lustre program

Lustre compiler

Distribution specifications

N communicating automata

(location one automaton for each computing location)
### Distribution specifications

<table>
<thead>
<tr>
<th>location name</th>
<th>assigned rates</th>
<th>inferred inputs &amp; outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>base</td>
<td>CK, RES</td>
</tr>
<tr>
<td>M</td>
<td>CK</td>
<td>IN, OUT</td>
</tr>
</tbody>
</table>

The inferred inputs and outputs are those whose rate matches the assigned rate.

### First attempt of distribution

**State 0 -- location L**

```plaintext
state 0
go(CK, IN)
if (CK) then
    RES := OUT
    V := OUT
    OUT := SLOW(IN)
    write(OUT)
else
    RES := V
endif
write(RES)
goto 1
```

**State 0 -- location M**

```plaintext
state 0
go(CK, IN)
if (CK) then
    RES := OUT
    V := OUT
    OUT := SLOW(IN)
    write(OUT)
else
    RES := V
endif
write(RES)
goto 1
```
First attempt of distribution

state 0 -- location L
  go(CK)
  if (CK) then
    RES:=OUT
    V:=OUT
  else
    RES:=V
  endif
  write(RES)
goto 1

state 0 -- location M
  go(IN)
  if (CK) then
    OUT:=SLOW(IN)
    write(OUT)
  else
    OUT:=SLOW(IN)
    write(OUT)
  endif
goto 1

The go(CK, IN) has been split into
  go(CK) on location L
  go(IN) on location M

The value of CK is sent by L to M at each cycle of the base rate.

location M runs at the speed of the base rate instead of CK.

If the communications take 1, then the global WCET is still 8.
How to improve this?

- We want location M to run at the speed of CK
  - This would give enough time for the computation of SLOW
  - For this, location L must not send CK to location M
    - We can use an existing bisimulation for detecting and suppressing branchings like if(CK) on location M
    - For this bisimulation to work, the go(IN) action must be moved inside the then branch on location M
      - Makes sense because IN is expected only when CK is true

- The two programs will be logically desynchronized

Moving the go downward

- Only the locations whose rate is not the base rate

A simple forward traversal of the program:

```plaintext
loc. M (rate CK) - state 0
  go(IN)
  if (CK) then
    OUT:=SLOW(IN)
    write(OUT)
    goto 1
  else
    goto 0
  endif
```

Moving the go downward

- Only the locations whose rate is not the base rate

A simple forward traversal of the program:

```plaintext
loc. M (rate CK) - state 0
  go(IN)
  if (CK) then
    go(IN)
    OUT:=SLOW(IN)
    write(OUT)
    goto 1
  else
    goto 0
  endif
```
Suppressing useless branchings

Bisimulation fully presented in [Caspi, Fernandez & Girault 1995]

state 0

if (CK)
go(IN)
write(OUT)
OUT:=SLOW(IN)
goto 1
goto 0

if (CK)
go(IN)
write(OUT)
OUT:=SLOW(IN)
goto 1

state 1

Suppressing useless branchings

Bisimulation fully presented in [Caspi, Fernandez & Girault 1995]

state 0

if (CK)
go(IN)
write(OUT)
OUT:=SLOW(IN)
goto 1

if (CK)
go(IN)
write(OUT)
OUT:=SLOW(IN)
goto 1
Final result

location \( L \) (rate base)

state 0:
go(CK)
if (CK) then {
  RES:=0
  write(RES)
  V:=0
  goto 1
} else {
  RES:=V
} endif

go(CK)

state 1:
go(IN)
OUT:=SLOW(IN)
RES:=OUT
V:=OUT
write(RES)
goto 1

location \( M \) (rate CK)

state 0:
go(CK)
if (CK) then {
  OUT:=receive(M)
  RES:=OUT
  V:=OUT
} else {
  RES:=V
} endif

go(IN)
OUT:=SLOW(IN)
write(RES)
goto 1

–p . 2 4 / 3 5
A run of the newly distributed FILTER

RES= 0 0 0 42 42 42 27 27 27
CK= T F F T F F T F F ...

logical time/state for \( L \)

\( \text{OUT}_1 = 42 \)
\( \text{OUT}_2 = 42 \)
\( \text{OUT}_3 = 27 \)
\( \text{OUT}_4 = 27 \)
\( \text{OUT}_5 = 27 \)

\( \text{IN}_1 = 13 \)
\( \text{IN}_2 = 9 \)
\( \text{IN}_3 = 40 \)
\( \text{IN}_4 = 69 \)

logical time/state for \( M \)

The period of \( L \) is one third of the period of \( M \)

Validating the synchronous abstraction

We have to compare the WCET with the execution loop period
But our program is distributed into \( n \) tasks. So:

- We compute the \( n \) WCET
- We compute the total utilisation factor
- We check the Liu & Layland conditions (mono-processor case)

Dummy communications can finally be added to guarantee bounded FIFO queues

A run of the newly distributed FILTER

–p . 2 5 / 3 5

–p . 2 6 / 3 5

–p . 2 5 / 3 5

–p . 2 5 / 3 5
Validating the synchronous abstraction

We have to compare the WCET with the execution loop period

But our program is distributed into \( n \) tasks. So:

- We compute the \( n \) WCET
- We compute the total utilisation factor
- We check the Liu & Layland conditions (mono-processor case)

<table>
<thead>
<tr>
<th>location</th>
<th>( L )</th>
<th>( M )</th>
</tr>
</thead>
<tbody>
<tr>
<td>WCET</td>
<td>2</td>
<td>8</td>
</tr>
<tr>
<td>rate</td>
<td>5</td>
<td>15</td>
</tr>
</tbody>
</table>

\[
\frac{2}{5} + \frac{8}{15} = \frac{14}{15} \leq 1
\]

RTOS implementation

\[
\text{logical time/state for } L
\]

\[
\text{logical time/state for } M
\]

\[
\text{logical time/state for } L
\]

\[
\text{logical time/state for } M
\]
This mechanism relies on the preemption mechanism of the RTOS!

Data-flow analysis

Program of location M

state 0:
go(IN)

OUT:=SLOW(IN)

write(OUT)
goto 1

state 1:
go(IN)

OUT:=SLOW(IN)

write(OUT)
goto 1

send(L,OUT)

state 0:
go(IN)

OUT:=SLOW(IN)

write(OUT)
goto 1

send(L,OUT)

state 1:
go(IN)

OUT:=SLOW(IN)

write(OUT)
goto 1

send(L,OUT)
Data-flow analysis

Program of location $M$

```
state 0:
go(IN)
OUT:=SLOW(IN)
write(OUT)
goto 1
send(L,OUT)
```

```
state 1:
go(IN)
OUT:=SLOW(IN)
write(OUT)
goto 1
send(L,OUT)
```

Clocks

Each flow has a **clock** (= *first class abstract type*)

- The sequence of instants where the flow bears a value

Any Boolean flow defines a new clock: the sequence of instants where it bears the value **true**

Flows can then be **up**sampled (*current*) and **down**sampled (*when*)

A program must be correctly clocked

One clock is called the **base clock** of the program:

- the sequence of its activation instants (the Esterel **tick**)

The set of clocks is a **tree** whose root is the base clock

Syntax

```
ode FILTER (CK : bool; (IN : int) when CK)
returns (RES : int; (OUT : int) when CK);
let
RES = current ((0 when CK) -> pre OUT);
OUT = SLOW (IN);
tel.
function SLOW (A : int) returns (B : int);
```

Two applications

1. Clock driven automatic distribution of Lustre programs

   Lustre is synchronous, declarative, data-flow

   All objects are **flows**: infinite sequences of **typed** data

2. Automatic rate desynchronisation of Esterel programs

   Clocks

   Each flow has a clock (= *first class abstract type*)

   - The sequence of instants where the flow bears a value

   Any Boolean flow defines a new clock: the sequence of instants where it bears the value **true**

   Flows can then be **up**sampled (*current*) and **down**sampled (*when*)

   A program must be correctly clocked

   One clock is called the **base clock** of the program:

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Syntax

node FILTER (CK : bool; (IN : int) when CK) returns (RES : int; (OUT : int) when CK);
let
RES = current ((0 when CK) -> pre OUT);
OUT = SLOW (IN);
tel.

function SLOW (A : int) returns (B : int);

The SLOW function is long duration task

An example of a run of FILTER

<table>
<thead>
<tr>
<th>base</th>
<th>clock</th>
<th>cycle number</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
</tr>
</thead>
<tbody>
<tr>
<td>CK</td>
<td></td>
<td></td>
<td>T</td>
<td>F</td>
<td>F</td>
<td>T</td>
<td>F</td>
<td>F</td>
<td>T</td>
<td>F</td>
<td>F</td>
</tr>
<tr>
<td>IN</td>
<td></td>
<td></td>
<td>14</td>
<td>9</td>
<td>23</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

base clock cycle number | 1   | 2   | 3   | 4   | 5   | 6   | 7   | 8   | 9   |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CK</td>
<td>T</td>
<td>F</td>
<td>F</td>
<td>T</td>
<td>F</td>
<td>F</td>
<td>T</td>
<td>F</td>
<td>F</td>
</tr>
<tr>
<td>IN</td>
<td>14</td>
<td>9</td>
<td>23</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OUT = SLOW(IN)</td>
<td>42</td>
<td>27</td>
<td>69</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### An example of a run of FILTER

<table>
<thead>
<tr>
<th>base clock cycle number</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>...</th>
</tr>
</thead>
<tbody>
<tr>
<td>CK</td>
<td>T</td>
<td>F</td>
<td>F</td>
<td>T</td>
<td>F</td>
<td>F</td>
<td>T</td>
<td>F</td>
<td>F</td>
<td></td>
</tr>
<tr>
<td>IN</td>
<td>14</td>
<td>9</td>
<td>23</td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pre OUT</td>
<td>nil</td>
<td>42</td>
<td>27</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 when CK</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(0 when CK) -&gt; pre OUT</td>
<td>0</td>
<td>42</td>
<td>27</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- RES = current (...) 000 42 42 42 27 27 27 ...
An example of a run of **FILTER**

<table>
<thead>
<tr>
<th>base clock cycle number</th>
<th>1 2 3 4 5 6 7 8 9 ...</th>
</tr>
</thead>
<tbody>
<tr>
<td>CK</td>
<td>T F F T F F T F F ...</td>
</tr>
<tr>
<td>IN</td>
<td>14 9 23 ...</td>
</tr>
<tr>
<td>OUT = SLOW(IN)</td>
<td>42 27 69 ...</td>
</tr>
<tr>
<td>pre OUT</td>
<td>nil 42 27 ...</td>
</tr>
<tr>
<td>0 when CK</td>
<td>0 0 0 ...</td>
</tr>
<tr>
<td>(0 when CK) -&gt; pre OUT</td>
<td>0 42 27 ...</td>
</tr>
<tr>
<td>RES = current (...)</td>
<td>0 0 0 42 42 42 27 27 27 ...</td>
</tr>
</tbody>
</table>

These are logical instants

**OUT** must be available at the same clock cycle of **CK** as **IN**

Clock-driven automatic distribution

Automatic distribution:

From a centralised source program and some distribution specifications, we build automatically as many programs as required by the user.

Their combined behaviour will be functionally equivalent to the behaviour of the initial centralised program.

**OUT** must be available at the same clock cycle of **CK** as **IN**

**RES** must be available at the next clock cycle of **CK**
Clock-driven automatic distribution

Automatic distribution:

From a centralised source program and some distribution specifications, we build automatically as many programs as required by the user.

Their combined behaviour will be functionally equivalent to the behaviour of the initial centralised program.

Clock-driven:

The user specifies which clock goes to which computing location.

Partition of the set of clocks of the centralised source program

One subset for each desired computing location.

Related work

- Giotto compiler: [Henzinger, Horowitz & Kirsch 2001]
- Asynchronous tasks in Esterel: [Paris 1992]
- Distributed implementation of Lustre over TTA: [Caspi, Curic, Maignan, Sofronis, Tripakis & Niebert 2003]
- Futures in Heptagon: [Gérard 2013]

Asynchronous tasks in Esterel

Tasks are external computation entities syntactically similar to procedures, but the execution of which is assumed to be non-instantaneous.

\begin{verbatim}
module FILTER:
  input CK;
  input IN : integer;
  output RES, OUT : integer;
  task SLOW(integer)(integer);
  return R;
loop
  present CK then
    exec SLOW(OUT)(IN) return R;
  else
    emit RES (pre(?RES))
  end present
||
  present R then
    RES = ?OUT;
  end present
end module
\end{verbatim}

Futures in Heptagon

A future is a computation the evaluation of which is launched concurrently, and the result of which is expected later.

\begin{verbatim}
node SLOW (A:int) returns (B:int)
let
do some computations();
tel

node FILTER (CK:bool, IN:int) returns (RES:int)
var OUT : future int;
let
  OUT = async SLOW (IN);
  RES = merge CK (!((async 0) fby OUT))
    (0 fby (RES whenot CK));
tel
\end{verbatim}
End of chapter 3