

# CAP - Exercises: static semantics (chapter 4: typing)

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## Abstract syntax

Recall the abstract syntax of the course for expressions :

$$\begin{array}{ll}
 e ::= & \text{constant} \\
 | & \text{variable} \\
 | & \text{addition} \\
 | & \text{multiplication} \\
 | & \dots
 \end{array}$$

and the mini-while language :

$$\begin{array}{ll}
 S(Smt) ::= & \text{assign} \\
 | & \text{do nothing} \\
 | & \text{sequence} \\
 | & \text{test} \\
 | & \text{loop}
 \end{array}$$

We expand the language with variable declarations :

$$D(\text{decl}) ::= \text{var } x : t \text{ type declaration}$$

We recall that environments associate a type to variables ( $\Gamma$ ). Here, the environment is constructed by the following rules :

### Declarations

$$\frac{\overline{\text{var } x : t \rightarrow_d [x \mapsto t]} \quad D_1 \rightarrow_d \Gamma_1 \quad D_2 \rightarrow_d \Gamma_2 \quad \text{Dom}(\Gamma_1) \cap \text{Dom}(\Gamma_2) = \emptyset}{D_1; D_2 \rightarrow_d \Gamma_1 \cup \Gamma_2}$$

**Expressions** Like in the course, for instance :

$$\frac{\Gamma \vdash e_1 : \text{int} \quad \Gamma \vdash e_2 : \text{int}}{\Gamma \vdash e_1 + e_2 : \text{int}}$$

**Commands** Like in the course, for instance :

$$\frac{\Gamma \vdash b : \text{boolean} \quad \Gamma \vdash S : \text{void}}{\Gamma \vdash \text{while } b \text{ do } S \text{ done} : \text{void}}$$

**And a program**

$$\frac{D \rightarrow \Gamma \quad \Gamma \vdash C : \text{void}}{\Gamma \vdash DC : \text{void}}$$

**EXERCISE ▶ Well typed**

Type the program :

```
var x1 : integer ; var x2 : integer ; var x3 : integer
x1 := 3 ;
while (not x3) do
  x1 := x2 + 1 ;
  x3 := x3 and true
done
```

**EXERCISE ▶ Expand expressions**

Complete the abstract syntax and the static semantics (typing) of expressions with the new construction  $e_1? e_2: e_3$ : if  $e_1$  is true then the expression has value  $e_2$  else  $e_3$ .

**EXERCISE ▶ Expand the statements**

Complete the abstract syntax and the static semantics (typing) of statements with an extended for :

```
for i in e1 .. e2 S
```

2 cases :

- The instruction declares the  $i$  variable (like in Ada)
- $i$  should be declared before.