PROC18 ISA - Documentation

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About

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— Document : Remy Grüblatt, Laure Gonnord, Sébastien Michelland, and Matthieu Moy, for CAP and MIF08.

This is a simplified version of the machine, which is (hopefully) conform to the chosen simulator.

1 Installing the simulator and getting started

To get the PROC18 assembler and simulator, follow instructions of the first lab (git pull on the course lab repository).

2 The PROC18 architecture

Among others, the PROC18 architecture has two particular features :

— The number of bits used to encode instructions is non constant. But for compilation, we do not care !

— Read and write instructions use special registers.

Here is an example of PROC18 assembly code for 2018 :

```
1   leti r0 17      ; initialisation of a register to 17
loop:
  sub2i r0 1        ; subtraction of an immediate
  jumpif nz loop    ; equivalent to jump xx
```

Memory, Registers The memory is adressed by bits (and not words), from address 0.

The PROC18 has 8 registers from r0 to r7. Only r7 [1] is reserved for the routine return address. There are specific registers ("counters") for manipulating memory, namely `a1` and `a0`. Finally, we have special registers `sp` (*Stack Counter*) and `pc` (*Program Counter*). Accesses to registers are direct, and Section 2 explains how to access memory.

Shifts The directions for the shift are either "left" or "right".

1. Registers are in lower case.

TABLE 1 – PROC18 instructions. For constants, padding is done with zeros (z) or sign extension (s).

opcode	mnemonic	operands	description	ext.	Flags update
0000	`add2`	*reg reg*	addition		zcvn
0001	`add2i`	*reg const*	add immediate constant	z	zcvn
0010	`sub2`	*reg reg*	subtraction		zcvn
0011	`sub2i`	*reg const*	subtract immediate constant	z	zcvn
0100	`cmp`	*reg reg*	comparison		zcvn
0101	`cmpi`	*reg const*	comparison with immediate constant	s	zcvn
0110	`let`	*reg reg*	register copy		
0111	`leti`	*reg const*	fill register with constant	s	
1000	`shift`	*dir reg shiftval*	logical shift		zcn
10010	`readze`	*ctr size reg*	read *size* memory bits (zero-extended) to *reg*		
10011	`readse`	*ctr size reg*	read *size* memory bits (sign-extended) to *reg*		
1010	`jump`	*addr*	relative jump		
1011	`jumpif`	*cond addr*	conditional relative jump		
110000	`or2`	*reg reg*	logical bitwise or		zcn
110001	`or2i`	*reg const*	logical bitwise or	z	zcn
110010	`and2`	*reg reg*	logical bitwise and		zcn
110011	`and2i`	*reg const*	logical bitwise and	z	zcn
110100	`write`	*ctr size reg*	write the lower *size* bits of *reg* to mem		
110101	`call`	*addr*	sub-routine call	s	
110110	`setctr`	*ctr reg*	set one of the four counters to the content of *reg*		
110111	`getctr`	*ctr reg*	copy the current value of a counter to *reg*		
1110000	`push`	*reg*	push value of register on stack		
1110001	`return`		return from subroutine		
1110010	`add3`	*reg reg reg*			zcvn
1110011	`add3i`	*reg reg const*		z	zcvn
1110100	`sub3`	*reg reg reg*			zcvn
1110101	`sub3i`	*reg reg const*		z	zcvn
1110110	`and3`	*reg reg reg*			zcn
1110111	`and3i`	*reg reg const*		z	zcn
1111000	`or3`	*reg reg reg*			zcn
1111001	`or3i`	*reg reg const*		z	zcn
1111010	`xor3`	*reg reg reg*			zcn
1111011	`xor3i`	*reg reg const*		z	zcn
1111100	`asr3`	*reg reg shiftval*			zcn
1111101	`sleep`		sleep		
1111110	`rand`		rand		
1111111	`lea`	*reg addr*	load effective address *addr*		
11111110	`print`	type *reg*	print		
11111111	`printi`	type *const*	print		

Flags Each instruction may update carry flags (last column of 1). Flags represent informations about the last operation that modified them :

- **z** : The result of the previous operation was a **z**ero.
- **c** : A **c**arry happened during the previous operation.
- **v** : An o**v**erflow happened during the previous operation.
- **n** : The result of the previous operation is strictly negative (¡0).

Check the file `cap-labs18/target18/doc/emu_flag_management.md` for details.

TABLE 2 – Constant encoding

addr : *prefix-free* encoding for addresses and moves	
0 + 8 bits	value of move on 8 bits
10 + 16 bits	same on 16 bits
110 + 32 bits	same on 32 bits
111 + 64 bits	same on 64 bits
shiftval : *prefix-free* encoding of shift constants	
0 + 6 bits	constant between 0 and 63
1	constant value 1
const : *prefix-free* encoding of ALU constants	
0 + 1 bit	constant 0 ou 1
10 + 8 bits	byte
110 + 32 bits	
111 + 64 bits	
size : *prefix-free* encoding of memory sizes	
00	1 bit
01	4 bits
100	8 bits
101	16 bits
110	32 bits
111	64 bits

Constants : `let` and `leti` These expressions provide ways to initialize or copy registers.

The constants are encoded according to 2 (encoding of ALU constants). For the `leti` instruction, padding is done with sign extension. Thus :

```
1  leti r0 −17
```

stores the constant -17 in register r0, and the encoding of the instruction is :

```
0111 000 1011101111
```

Register copy is done with :

```
let r0 r1
```

Arithmetical and logical instructions Arithmetical and logical instructions have 2 or 3 operands :

```
add3i r1 r0 3     ; r1 <− r0+3
add2i r1 15       ; r1 <− r1+15
add3 r1 r2 r3     ; r1 <− r2+r3
4  add2 r1 r2     ; r1 <− r1+r2
```

The first operand is always the destination register, and the two remaining operands are sources, registers or constants. If a constant is used then its value is encoded in the instruction following the encoding depicted in Table 2. For instance :

```
1  add2i r1 15       ; r1 <− r1+15
```

is encoded as :

```
0001 001 10 00001111 ;
add2i, register 1, 1 byte constant (*addr* prefix code), value 15 and padding with 0
```

Be careful, `add` only uses positive constants :

TABLE 3 – Tests

			mnemonic	description (after `cmp` op1 op2)
0	0	0	`eq`, `z`	equal, op1 = op2
0	0	1	`neq`, `nz`	not equal, op1 ≠ op2
0	1	0	`sgt`	signed greater than, op1 > op2, two's complement
0	1	1	`slt`	signed smaller than, op1 < op2, two's complement
1	0	0	`sge`	op1 ≥ op2, signed
1	0	1	`ge`, `nc`	op1 ≥ op2, unsigned
1	1	0	`lt`, `c`	op1 < op2, unsigned
1	1	1	`sle`	op ≤ op2, signed

add3i r1 r0 −12

Throw the following error :

```
couldn't read UCONSTANT : The value is not in the right range
```

Branching (`jump` `jumpif`) Let `a` be the address of the instruction following the `jump` or `call` instruction, and `c` the integer encoded in a constant of type *addr* (see Table 2), and signed.

The `jump` instruction executes `pc` ← `a` + `c`.

The `jumpif` instruction does the same, but only if the condition is true (see Section 2).

The `call` instruction stores R7 in PC and jumps to the called address.

The `return` instruction does `pc` ← *R*7.

In :

---

loop:
sub2i r0 1 *; substraction of an immediate*
jumpif nz loop *; equivalent to jump −25*

---

is assembled into

```
0011 000 01                      ; 9 bits
1011 001 011100111               ; 16 bits
jump, nz, 0 (mv on 8 bits), -25 bits jump
```

Tests Operands 1 and 2 are encoded like in the ALU instructions. In particular the second operand can be an immediate constant. The condition is encoded thanks to Table 3.

In this class, we will use only the signed version of comparisons (`sgt`/`slt`/`sle`/`sge`, and `eq`/`neq`/`z`/`nz` which work for both signed and unsigned). Not all unsigned comparisons are available, and they are misleading : don't use them here.

Memory accesses Special registers `a0`, `a1` are used to access memory.

The instructions `readze`, `readse` and `write` read or write the specified number of bits and also increment the associated (address) registers :

readze a0 4 r1

reads 4 bits of memory content from the address stored in `a0` and store them in `r1` (with a zero padding). In addition, `a0` is incremented by 4.

write a1 2 r1

Table 4 – Counters (special registers).

encoding	mnemonic	description
00	`pc`	program counter
01	`sp`	stack pointer
10	`a0`	generic address counter
11	`a1`	generic address counter

writes the lower 2 bits of register `r1`.

We can emulate the classical read operation in memory from an adress stored in a register $r_2 \leftarrow Mem[r_1]$:

```
setctr a0 r1
readse a0 xxx r2 ; xxx the number of bits to read
```

The instruction `lea r3 label` loads the address corresponding to label onto r3. For instance, the following program :

```
    lea r0 foo

3 foo:
    .const 5 #10101
```

loads the adress of the constant. The `#` prefix is used to introduce a binary constant (10101, i.e. 21), and works only for the `.const` directive. It is assembled into :

```
11111101 000 000000000
10101
```

The PROC18 emulator's memory layout is documented in the `cap-labs18/target18/doc/emu_memory_layout.md` file.

Print Two examples of use of the native print instruction :

```
1   let   r0 126
    print char r0       ; "~"
    print char '\n'     ; newline
    print signed r0     ; "126"
    print unsigned r0   ; "0x7e"
6   print unsigned '0'  ; "0x30"
```

You can also print a string at a given label with :

```
    lea   r0 str
    print string r0     ; "Hello, World!"

4 str:
    .string "Hello, World!"
```

Assembly directives A bit more of syntax :

— The assembly begins at address 0.
— Labels can be used for jumps.
— The keyword `.const n xxxx` reserves a memory cell initialized to the n bits constant xxxx.
— The keyword `.string ''Hello''` reserves 6 memory cells and store the ascii numbers corresponding to all the characters of the message (ending it with a Null character).
— Hexadecimal constants are prefixed by `0x`, for instance `0xff` is decimal 255.
— Comments begin with a semicolum `;`

The assembly implements a stack in memory, from an address stored in the special register `sp`. We will use it in Lab5.

Stopping execution When instructions terminate, the emulator halts the execution. But as it has no way of differenciating instructions from data (like strings or constants), the emulator provides a way to stop execution by detecting infinite self loops, such as this one :

```
halt:
    jump halt
```

3 Help to encode constants

hex to binary

a	b	c	d	e	f
1010	1011	1100	1101	1110	1111

2's complement Let us code $n = (-3)_{10}$ in 2's complement on 6 bits, with the recipe : "code -n in base 2, then negate bitwise, then add one". First, 3 is encoded as `000011` on 6 bits. Its negation is `111100`, thus $(-3)_{10} = \texttt{111101}_{\bar{2}}$.